

CLAIMS

What is claimed is:

1 1. In an amplifier system, a method for amplifying an input signal to generate an amplified output
2 signal, comprising:

3 generating the amplified output signal using an amplifier path of the amplifier system;

4 generating a reference signal using a reference path of the amplifier system;

5 combining a sample of the amplified output signal and a sample of the reference signal to form a
6 combined signal;

7 detecting power level of the combined signal; and

8 controlling operations of the amplifier path based on the detected power level, wherein overall signal
9 delay of the amplifier path does not match overall signal delay of the reference path.

1 2. The invention of claim 1, wherein the power level of the combined signal is detected at a selected
2 frequency corresponding to cancellation between the amplified output signal and the reference signal.

1 3. The invention of claim 2, wherein the selected frequency corresponds to a frequency present in
2 the input signal.

1 4. The invention of claim 2, wherein:

2 the reference signal corresponds to a pilot tone that is also injected into the amplifier path; and

3 the selected frequency corresponds to the frequency of the pilot tone.

1 5. The invention of claim 2, further comprising changing the selected frequency over time.

1 6. The invention of claim 5, wherein the selected frequency is changed to achieve a different phase
2 or gain insertion for the amplifier path.

1 7. The invention of claim 5, wherein the selected frequency is changed to compensate for changes
2 in operating characteristics of the amplifier system.

1 8. The invention of claim 5, wherein the selected frequency is changed based on changes in
2 frequency of the input signal.

1 9. The invention of claim 1, wherein controlling the operations of the amplifier path comprises
2 controlling at least one of phase and delay of the amplifier path.

1 10. The invention of claim 9, wherein controlling the operations of the amplifier path further
2 comprises controlling gain of the amplifier path.

1 11. The invention of claim 1, wherein the reference path is implemented without a delay element that
2 nominally equalizes overall delay offset between the amplifier and reference paths.

1 12. The invention of claim 11, wherein the reference path comprises a delay element such that the
2 overall signal delay of the reference path is larger than the overall signal delay of the amplifier path.

1 13. The invention of claim 1, wherein the reference path is implemented with a variable delay or
2 phase element to controllably change overall delay or phase offset between the amplifier and reference
3 paths.

1 14. The invention of claim 1, wherein the combined signal is formed from a summation of the
2 amplified output signal sample and the reference signal sample.

1 15. An amplifier system for amplifying an input signal to generate an amplified output signal, the
2 amplifier system comprising:

3 an amplifier path adapted to generate the amplified output signal from the input signal;
4 a reference path adapted to generate a reference signal;
5 a node adapted to generate a combined signal from a sample of the amplified output signal and a
6 sample of the reference signal;
7 a power detector adapted to detect power level of the combined signal; and
8 a controller adapted to control operations of the amplifier path based on the detected power level,
9 wherein overall signal delay of the amplifier path does not match overall signal delay of the reference
10 path.

11 16. The invention of claim 15, wherein the power detector is adapted to detect the power level of the
12 combined signal at a selected frequency corresponding to cancellation between the amplified output
13 signal and the reference signal.

1 17. The invention of claim 16, wherein the selected frequency corresponds to a frequency present in
2 the input signal.

1 18. The invention of claim 16, further comprising a pilot tone generator adapted to generate a pilot
2 tone that is injected into the amplifier and reference paths, wherein the selected frequency corresponds to
3 the frequency of the pilot tone.

1 19. The invention of claim 18, wherein the controller is adapted to control operations of the pilot
2 tone generator to change the frequency of the pilot tone.

1 20. The invention of claim 16, wherein the controller is adapted to change the selected frequency of
2 the power detector over time.

1 21. The invention of claim 20, wherein the controller is adapted to change the selected frequency to
2 achieve a different phase or gain insertion for the amplifier path.

1 22. The invention of claim 20, wherein the controller is adapted to change the selected frequency to
2 compensate for changes in operating characteristics of the amplifier system.

1 23. The invention of claim 20, wherein the controller is adapted to change the selected frequency
2 based on changes in frequency of the input signal.

1 24. The invention of claim 15, wherein:
2 the amplifier path further comprises at least one of a variable phase adjuster adapted to adjust phase
3 of the amplified output signal and a variable delay adjuster adapted to adjust delay of the amplified
4 output signal; and
5 the controller is adapted to control operations of the at least one of the variable phase adjuster and the
6 variable delay adjuster.

1 25. The invention of claim 24, wherein:
2 the amplifier path further comprises a variable amplitude adjuster adapted to adjust amplitude of the
3 amplified output signal; and
4 the controller is further adapted to control operations of the variable amplitude adjuster.

1 26. The invention of claim 15, wherein the reference path is implemented without a delay element
2 that nominally equalizes overall delay offset between the amplifier and reference paths.

1 27. The invention of claim 26, wherein the reference path comprises a delay element such that the
2 overall signal delay of the reference path is larger than the overall signal delay of the amplifier path.

1 28. The invention of claim 15, wherein the reference path comprises a variable delay or phase
2 element adapted to controllably change overall delay or phase offset between the amplifier and reference
3 paths.

4 29. The invention of claim 28, wherein the controller is adapted to control operations of the variable
5 delay or phase element.

1 30. The invention of claim 15, wherein the node is adapted to form the combined signal from a
2 summation of the amplified output signal sample and the reference signal sample.

1 31. The invention of claim 15, wherein the amplifier system is implemented in a single integrated
2 circuit.

1 32. An integrated circuit having an amplifier system for amplifying an input signal to generate an
2 amplified output signal, the amplifier system comprising:

3 an amplifier path adapted to generate the amplified output signal from the input signal;

4 a reference path adapted to generate a reference signal;

5 a node adapted to generate a combined signal from a sample of the amplified output signal and a
6 sample of the reference signal;

7 a power detector adapted to detect power level of the combined signal; and

8 a controller adapted to control operations of the amplifier path based on the detected power level,
9 wherein overall signal delay of the amplifier path does not match overall signal delay of the reference
10 path.

1 33. An amplifier system for amplifying an input signal to generate an amplified output signal, the
2 amplifier system comprising:

3 an amplifier path adapted to generate the amplified output signal from the input signal;

4 a reference path adapted to generate a reference signal;

5 a node adapted to generate a combined signal from a sample of the amplified output signal and a
6 sample of the reference signal;
7 a power detector adapted to detect power level of the combined signal; and
8 a controller adapted to control operations of the amplifier path based on the detected power level,
9 wherein the reference path is implemented without a delay element that nominally equalizes overall delay
10 offset between the amplifier and reference paths.